

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	§	
Juan-Antonio Carballo	§	
	§	Group Art Unit: Not Yet Assigned
Serial No.: Not Yet Assigned	§	
	§	Examiner: Not Yet Assigned
Date Filed: Herewith	§	IBM Docket No.: AUS920030890US1
	§	Intellectual Property Law Dept.
Title: Methods and Arrangements for	§	International Business Machines Corp.
Link Power Reduction	§	11400 Burnet Road
	§	Austin, Texas 78758

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit herewith patents, publications, or other information of which they are aware, which they believe may be material to the patentability of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR 1.56.

While this Information Disclosure Statement may be “material” pursuant to 37 CFR 1.56, it is not intended to constitute an admission that any patent, publication, or other information referred to herein is “prior art” for this invention unless specifically designated as such.


In accordance with 37 CFR 1.97(g) the filing of this information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists.

The attached form, PTO-1449, provides a listing of patents, publications, or other information as required by 37 CFR 1.98(a)(1).

A copy of each of the items on PTO-1449, except published U.S. applications and patents, is supplied herewith.

Respectfully submitted,

Date: Dec. 22, 2003

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Completion if Known	
		Application Number	Not Yet Assigned
		Filing Date	Herewith
		First Named Inventor	Juan-Antonio Carballo
		Art Unit	Not Yet Assigned
		Examiner Name	Not Yet Assigned
Sheet 1	of 1	Attorney Docket Number	AUS920030890US1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		KUN JUNG CHANG, ET AL., 50 GB/S 32X32 CMOS Crossbar Chip Using, VLSI Circuits Issue Digest of Technical Papers, 1999, pp. 17-19.	
		M. J. LEE, ET AL., 84 -m W 4-Gb/s Clock and Data Recovery Circuit for Serial Link Applications, Symp[osium on VLSI Circuits Issue Digest of Technical Papers, 2001, pp. 149-152.	
		J.M. KHOURY, ET AL., High Speed Serial Transceivers for Data, IEEE Communications Magazine, Issue July 2001, Vol. 39, Issue 7, pp. 160-165.	
		R. FARJAD-RAD, et al., C. 3-M CMOS 8 Gigabit/S 4-PAM Serial Link, IEEE Journal of Solid State Circuits, Issue May 2000, pp. 757-764.	
		W. DALLY, ET AL., Transmitter Equal for 4 Gbits/Second Sig., Proc Hot Interconnects Symposium, Issue August 1996, pp. 29-39.	
		C.K. KEN YANG, ET AL., 0.5 M CMOS 4GB/S Serial Link Transceiver, IEEE Journal of Solid State Circuits, Issue May 1998, pp. 713-722.	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

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